A Temperature Noise Model for Extrinsic FETs

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Abstract—**A resistor temperature noise model for FETs has been successfully applied to extrinsic FETs to predict the frequency dependence of minimum noise figure, F_{min}, and associated gain, $G_{A\,opt}$. The model gives a fixed relationship between F_{min} and $G_{A\,opt}$, with one fitting parameter T_d. An extensive comparison to published results shows that the majority of FETs can be modelled with effective T_d values (the temperature of the output resistor) between 300 and 700 K for all of frequencies (8 to 94 GHz), gate lengths (0.8 to 0.1 μm) and material types examined. The analysis shows that InP-based MODFETs exhibit significantly lower F_{min} and higher $G_{A\,opt}$ than conventional and pseudomorphic GaAs-based MODFETs of the same gate length. The results suggest a high f_{max} is a key factor for low noise figure.**

I. Introduction

THIS paper gives a simple model for comparing published noise figure results of different types of FETs, measured at different frequencies. The noise of the extrinsic FETs is modelled with the effective thermal noise for the input and output resistors of the FET, as shown in Fig. 1. This noise model for extrinsic FETs is based on the resistor temperature model proposed for intrinsic FETs [1]. The intrinsic FET noise model accurately predicted all the noise parameters and their frequency dependence. However, the intrinsic model can not be applied to most published results because they generally do not provide accurate circuit models or full noise parameters. Furthermore, many published circuit models do not have physically reasonable element values. The extrinsic noise model is like a simple extrinsic FET circuit model [2], that is inadequate for accurate amplifier design at high frequencies, but is useful for circuit design concepts and comparisons of results at frequencies much less than f_{max}. The extrinsic T_d can be used like the extrinsic C_{gs}. A circuit designer matches the extrinsic C_{gs}, despite knowing that it is smaller than the intrinsic C_{gs} by a factor of approximately $1/(1 + g_m \cdot R_s)$ and that it is a non-physical capacitance. Similarly, the extrinsic T_d is smaller than the intrinsic T_d (the ratio of the T_ds is approximately the same as the ratio of the intrinsic and extrinsic f^2_{max}s) and the circuit designer may use the extrinsic T_d to estimate noise parameters when accurate noise models are not available.

The extrinsic noise model must be simple because most papers only give two noise parameters: the minimum noise figure, F_{min}, and the associated gain, $G_{A\,opt}$. Consequently the model can only have two fitting parameters. The fitting parameters are T_d, the effective noise temperature of the output resistor and f_{max}. This extrinsic model assumes that the input resistor noise temperature, T_g, is ambient and the noise currents due to T_g and T_d are uncorrelated. Despite being a simple model, it predicts the frequency dependence of F_{min} and $G_{A\,opt}$. When an f_{max} is given in a paper, the f_{max} extracted from the noise data with this extrinsic model is shown to agree well. The effective T_d, is remarkably consistent for a wide variety of FETs and measurement frequencies. T_d extracted for the extrinsic model is considered as a fitting parameter, like the Fukui fitting factor, K_f, and the effective T_d may have no physical significance. The effective T_d of the extrinsic FET can be used like the effective velocity given by $2\pi \cdot f_T \cdot L_g$, which is much less than the physical electron saturation velocity, but it is useful for comparing FETs.

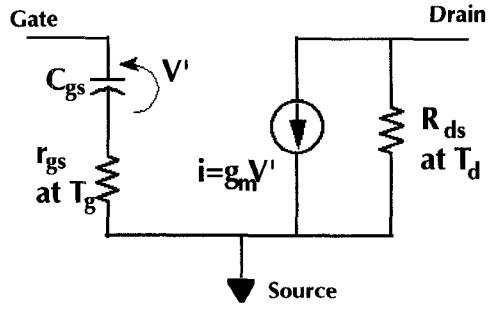

Fig. 1. Equivalent circuit of the intrinsic FET for the noise model.

The extrinsic model shows that there are relationships between F_{min} and $G_{A\,opt}$. The model is used as a framework to compare MODFET noise figures. The model and the results of the comparison suggest a higher f_{max} is important for a lower F_{min}. Finally, the model and comparisons lead to a discussion of designing FETs for lower noise figure and or achieving noise figure goals.

II. Noise Temperature Model

The expressions for the normalized noise parameters and $G_{A\,opt}$ of an intrinsic FET given in reference 1 are written here in a simpler form as functions of only T_g, T_d, f_{max} and T_{min}. Noise is expressed in terms of the effective, input, minimum noise temperature, T_{min}, rather than F_{min} for the temperature noise model.

$$T_{min} = (T_g T_d)^{1/2} \frac{f}{f_{max}} \left(\left(1 + \frac{T_d}{4T_g} \left(\frac{f}{f_{max}} \right)^2 \right)^{1/2} + \left(\frac{T_d}{4T_g} \right)^{1/2} \frac{f}{f_{max}} \right) \approx (T_g T_d)^{1/2} \frac{f}{f_{max}} \quad (1)$$

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$$G_{A\,\mathrm{opt}} = \frac{4r_{gs}\,G_{A\,\max}}{R_{\mathrm{opt}}\left(1+\frac{r_{gs}}{R_{\mathrm{opt}}}\right)^2} = \frac{2T_d}{T_{\min}}\,\frac{1+\frac{T_{\min}}{2T_g}}{1+\frac{T_{\min}}{T_g}} \approx \frac{2T_d}{T_{\min}} \tag{2}$$

$$G_{A\,\mathrm{opt}} = \frac{2T_{\min}}{T_g}\left(\frac{f_{\max}}{f}\right)^2 \frac{\left(1+\frac{T_{\min}}{2T_g}\right)}{\left(1+\frac{T_{\min}}{T_g}\right)^2} \approx \left(\frac{4T_d}{T_g}\right)^{1/2}\frac{f_{\max}}{f}$$

$$= \frac{f_{\mathrm{opt}}}{f} \tag{3}$$

$G_{A\,\max}$ of the intrinsic FET has the usual definition with respect to $f_{\max}$ and the circuit model shown in Fig. 1. An expression for the new parameter f_{opt} is obvious from inspection.

$$G_{A\,\max} = \left(\frac{f_{\max}}{f}\right)^2 = \frac{f_T^2}{4r_{gs}\,G_{ds}\,f^2}. \tag{4}$$

The other noise parameters for the extrinsic FET are the generator impedance for minimum noise figure, Z_{opt} ($R_{\mathrm{opt}} + jX_{\mathrm{opt}}$), and a normalized parameter, $\boldsymbol{n}$, used to describe the size of noise circles. R_{opt} is normalized to the input resistance, r_{gs}. X_{opt} is $j/(2\pi f C_{gs})$ [1]. The relationship of $\boldsymbol{n}$ to the familiar noise circle parameters R_n and N are also given.

$$\frac{R_{\mathrm{opt}}}{r_{gs}} = \frac{2T_g}{T_{\min}} + 1 \approx \left(\frac{4T_g}{T_d}\right)^{1/2}\frac{f_{\max}}{f} \tag{5}$$

$$\boldsymbol{n} = \frac{4\cdot N\cdot T_o}{T_{\min}} = \frac{4T_o R_{\mathrm{opt}} R_n}{T_{\min}|Z_{\mathrm{opt}}|^2} = \frac{2+\frac{T_{\min}}{T_g}}{1+\frac{T_{\min}}{T_g}} \approx 2. \tag{6}$$

The approximation for each of the expressions is for $T_{\min}$ much less than T_g (e.g., $F_{\min}$ less than 1.5 dB), which is also for frequencies much less than $f_{\max}$. The accuracy of the expressions at predicting $T_{\min}$ and $G_{A\,\mathrm{opt}}$ for extrinsic FETs as a function of frequency is shown in this paper.

III. Minimum Noise Temperature

The approximate expression for $T_{\min}$ predicts that $T_{\min}$ increases linearly with frequency, f. This low frequency approximation is compared to the full equation in Fig. 2 for a T_g of 298 K and an effective output resistor noise temperature, T_d, of 500 K. Later in this paper it is shown that 500 K is a typical T_d for an extrinsic FET model, independent of frequency and FET type. This model suggests that a key to a lower noise figure is a higher $f_{\max}$.

Also shown in Fig. 2 are experimental results for 0.25 μm AlGaAs/GaAs MODFETs over a wide frequency range of 8 to 62 GHz [3], [4]. Note that the data follows the change in slope predicted by theory. The best fit of the model to experimental $T_{\min}$ and $G_{A\,\mathrm{opt}}$ data is with a T_d of 534 K and $f_{\max}$ of 127 GHz. However, the typical T_d value, 500 K, fits well, as shown in Fig. 2. The model value of $f_{\max}$ agrees well with the $f_{\max}$ reported in the reference [3]: 135 GHz. The maximum difference between the measurements and the model is 0.16 dB at 62 GHz.

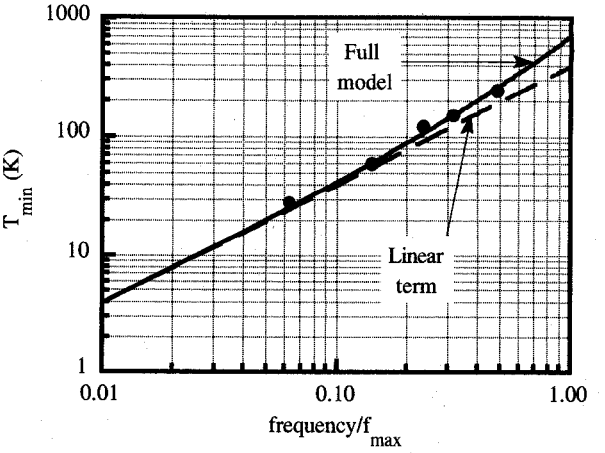

Fig. 2. Plot of $T_{\min}$ and the low frequency approximation for $T_{\min}$ versus frequency normalized to $f_{\max}$ for a T_g of 298 K and a T_d of 500 K. The full model is from equation (1) and the linear term is from the approximation to equation (1). ● experimental data [3].

A comparison of (1) with the Fukui equation [28], [29] shows that the Fukui fitting factor, K_f, is equal to $\sqrt{(4T_g T_d/(T_o^2 G_v))}$, where G_v is the FET voltage gain. This suggests that, lowering G_{ds} and increasing voltage gain g_m/G_{ds}, will reduce noise figure. Evidence for this is discussed in Section VI.

IV. Available Gain

The dependence of $G_{A\,\mathrm{opt}}$ on frequency given in (3) is shown in Fig. 3 for a T_d of 500 K and T_g of 298 K. The $G_{A\,\mathrm{opt}}$ plot shown in Fig. 3 has two slopes. As the operating frequency approaches $f_{\max}$, the FET gain is low and the input must be matched to maximize the signal from the generator compared to the output noise. Consequently, $G_{A\,\mathrm{opt}}$ approaches $G_{A\,\max}$ and $G_{A\,\mathrm{opt}}$ decreases at 6 dB per octave.

At frequencies much less than $f_{\max}$, $G_{A\,\mathrm{opt}}$ decreases at 3 dB per octave because R_{opt}/r_{gs} is proportional to $1/f$ and $G_{A\,\max}$ is proportional to $1/f^2$, as seen from the approximate expression for the noise parameters ((4) and (5)). The low frequency approximation for $G_{A\,\mathrm{opt}}$, f_{opt}/f, is compared to the full model in Fig. 3. For the example f_{opt} is 2.6 $f_{\max}$. The slope of $G_{A\,\mathrm{opt}}$ changes from $1/f$ to $1/f^2$ at 0.38 $f_{\max}$. At the break frequency R_{opt}/r_{gs} is $\sqrt{17}$ independent of T_d, T_g and $f_{\max}$for intrinsic FETs (uncorrelated noise temperatures) and the $G_{A\,\mathrm{opt}}$ is 6.6 dB at the break frequency.

Experimental data is also shown on Fig. 3 for 0.25 μm MODFETs measured at frequencies from 8 to 62 GHz [3], [4]. This gain data corresponds to the noise temper-

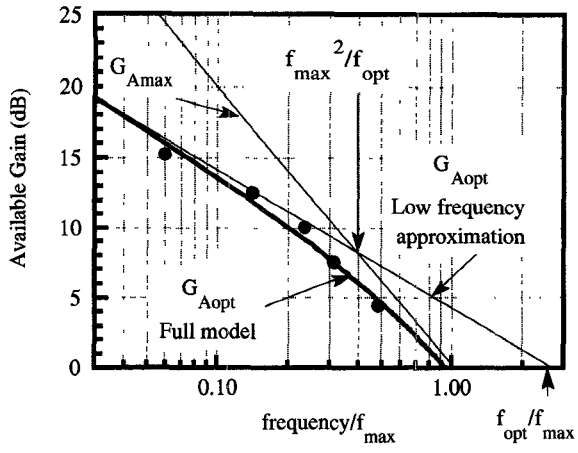

Fig. 3. Plot of the $G_{A\,opt}$ $G_{A\,opt}$ and the low frequency approximation to $G_{A\,opt}$ versus frequency normalized to f_{max} for a T_g of 298 K and T_d of 500 K. ● experimental data [3].

ature data shown in Fig. 2. Note that the gain data follows the slope change predicted by the model. The maximum error between the measured and modelled data is 0.9 dB at 30 GHz. The fit is excellent considering the uncertainties in tuning these amplifiers for minimum noise at mm-wave frequencies and the typical device-to-device non-uniformity.

The product of $G_{A\,opt}$ and T_{min} has a simple exact form for an intrinsic FET, where the noise temperatures are uncorrelated.

$$G_{A\,opt}\,T_{min} = T_d\,\boldsymbol{n} \tag{7}$$

The product $G_{A\,opt} \cdot T_{min}$ has a weak frequency dependence because $\boldsymbol{n}$ has a weak frequency dependence (see (6)). T_{min} is proportional to frequency and $G_{A\,opt}$ is inversely proportional to frequency for low T_{min} (T_{min} less than 120 K). Therefore, $G_{A\,opt}$ is proportional to $1/T_{min}$ at low T_{min}. Equation (7) can be explained qualitatively. The effective input noise power (for a 1 Hz bandwidth), kT_{min}, amplified by the available gain of the FET, can be considered as the total effective output noise power, $kT_{min} \cdot G_{A\,opt}$. Equation (7) shows that the effective total output noise power is approximately twice the noise power from the output resistor, $2kT_d$, because $\boldsymbol{n}$ approaches 2 for small T_{min}. Therefore, there are equal contributions from the output and input noise sources of a low-noise FET when the generator impedance is tuned for minimum noise.

The frequency independence of $G_{A\,opt} \cdot T_{min}$ for low noise FETs has been observed experimentally [5]. Asia [5] misinterpreted the frequency independence to imply that intrinsic (or output) noise source dominated the noise figure of FETs and that parasitic resistance (input thermal noise) contributed less noise than the intrinsic FET. A constant $G_{A\,opt} \cdot T_{min}$ product means that the total output noise power generated by the FET is independent of frequency. A decrease of parasitic resistance (e.g., R_s and R_g) reduces T_{min}, but also increases f_{max} and $G_{A\,opt}$. The $T_{min} \cdot G_{A\,opt}$ product changes very little because the changes of T_{min} and $G_{A\,opt}$ are in opposite directions. The $T_{min} \cdot G_{A\,opt}$ product is only a weak function of the parasitic resistances because $\boldsymbol{n}$ is only a weak function of f_{max} (see (6)).

The temperature noise model can be used not only to predict a $G_{A\,opt}$ and T_{min}, but also to extract an effective $G_{A\,max}$ and T_d by transposing equations 1 and 2. The expression for calculating an effective $G_{A\,max}$ and f_{max} is

$$G_{A\,max} = \left(\frac{f_{max}}{f}\right)^2 = \frac{T_g\,G_{A\,opt}}{2T_{min}} \frac{\left(1 + \dfrac{T_{min}}{T_g}\right)^2}{1 + \dfrac{T_{min}}{2T_g}} \approx \frac{T_g\,G_{A\,opt}}{2T_{min}} \tag{8}$$

The approximate expression also shows that $G_{A\,opt}/G_{A\,max}$ is simply $2T_{min}/T_g$ for low-noise FETs. An expression for calculating the effective T_d as function of T_{min} and G_{Aopt} from noise measurements is similar to (7):

$$T_d = \frac{T_{min}\,G_{A\,opt}}{2} \frac{1 + \dfrac{T_{min}}{T_g}}{1 + \dfrac{T_{min}}{2T_g}} \approx \frac{T_{min}\,G_{A\,opt}}{2} \tag{9}$$

These equations are applied to published noise data in the next section.

V. Comparison to the Literature

The minimum noise figure and available gain of a wide variety FETs reported in more than 60 references have been compared to the noise temperature model. The comparison includes FETs with gate lengths from 0.1 to 0.8 μm and different material types over a frequency range of 4 to 94 GHz. The results are summarized in the appendix in tables for conventional AlGaAs/GaAs MODFETs, AlGaAs/InGaAs pseudomorphic MODFETs, AlInAs/InGaAs MODFETs on InP substrates and GaAs MESFETs. An effective T_d and f_{max} were calculated from the F_{min} and $G_{A\,opt}$ reported in each paper. The comparison is limited to the minimum noise figure and available gain because there are few reports of the full noise parameters in the literature.

Plots of $G_{A\,opt}$ versus F_{min} are shown for each type of FET (Figs. 4 and 5). The data follows a curve similar to the modelled curves shown. Most of the data can be fitted with T_d values between 300 and 700 K. This small range of T_d is surprising because these are FETs of different material types and gate lengths and because the measurements are made over a wide range of frequencies. The limited range of T_d is useful for predicting noise parameters and identifying bad noise measurements or unusual FET designs. The relationship between $G_{A\,opt}$ and T_{min} given in (7) suggests that the plots should be T_{min} versus $G_{A\,opt}$ expressed in dB on a log-linear scale to obtain a straight line approximation at low noise figures. Noise data is usually given as F_{min} in dB. Fortunately, it can be shown F_{min} in dB is linearly proportional to f_{min} for F_{min} less than 4 dB. Consequently, the most useful plot is F_{min}

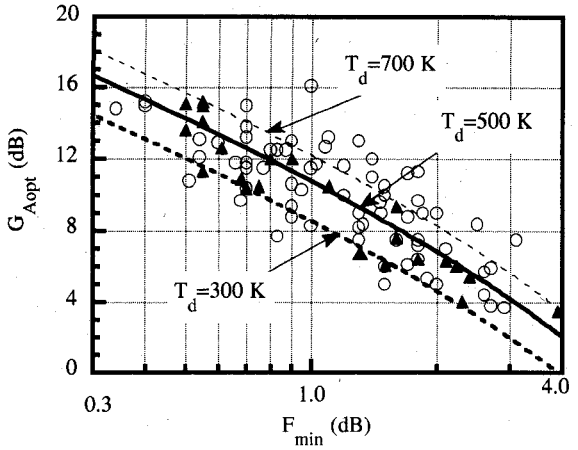

Fig. 4. Plot of the GA versus F_{min} published data of ○ conventional AlGaAs/GaAs and ▲ AlGaAs/InGaAs pseudomorphic MODFETs. The lines are the theory (equation 7) for a T_g of 298 K and T_d of 300, 500, and 700 K.

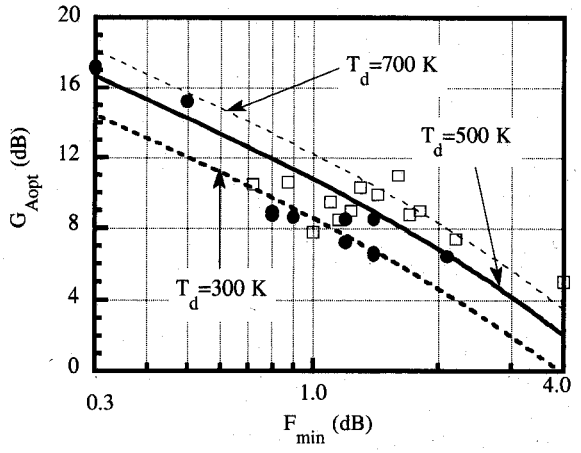

Fig. 5. Plot of the $G_{A\,opt}$ versus F_{min} for published data of ● AlInAs/InGaAs InP-based MODFETs and □ GaAs MESFETs. The lines are the theory (equation 7) for a T_g of 298 K and T_d values of 300, 500, and 700 K.

expressed in dB versus $G_{A\,opt}$ expressed in dB on a log-linear scale. The extrinsic noise model predicts $G_{A\,opt}$ is inversely proportional to F_{min} in dB until F_{min} approaches 4 dB, as shown in Figs. 4 and 5.

To help understand and compare the data given in the appendices, figures-of-merit were calculated for each result and the averages and percentage standard deviations of these figures-of-merit for the different types of FET are given in Table I. All the parameters have quite large standard deviations. Consequently, there is little confidence in distinguishing small differences between FET types.

All four types of FETs had similar average T_d values. There are not many InP-based MODFET results and the average T_d may be too high for these MODFETs because of potential errors measuring these extremely low-noise FETs at 18 GHz. f_{max} should scale with $1/L_g$ for well designed FETs [38], so the second parameter given in Table I is the $f_{max} \cdot L_g$ product. This product is significantly higher for InP-based MODFETs and this must be an important reason for the outstanding noise performance of these FETs (e.g., F_{min} of 0.8 dB at 60 GHz with a $G_{A\,opt}$ of 8.9 dB [6]).

Two factors, $F_{min}/f/L_g$ and $G_{A\,opt} \cdot f \cdot L_g$, are used as figures-of-merit. Values for these figures-of-merit are shown in the appendices and all tables. For low-noise FETs, these figures-of-merit should be approximately independent of frequency and gate length, if T_d is constant and f_{max} is scaled proportional to $1/L_g$. A similar noise figure factor was suggested by Goronkin and Nair [18]. The noise figure factor calculated in 1985 for conventional MODFETs was 0.228 dB/GHz/μm and this has not changed significantly for more recent publications. $F_{min}/f/L_g$ values calculated for pseudomorphic MODFETs are also similar to this value, as shown in Table I; only the InP-based MODFETs have a significantly better performance.

Differences between the figures-of-merit given in the appendices are observed. It is interesting to return to the original paper to understand the reasons for the variations. Differences between labs (or applications) are observed. Progress in device technology is seen. The summary of results shows that the same noise results are frequently published more than once. Unusual results are identified [19] and the original papers are reviewed to look for possible causes.

It is commonly believed that pseudomorphic MODFETs have the same noise figure as conventional MODFETs, but higher gain. However, the published data presented in Fig. 4 do not in general support this belief. The average $f_{max} \cdot L_g$ product is similar for AlGaAs/InGaAs pseudomorphic MODFETs, conventional AlGaAs MODFETs, and GaAs MESFETs at low noise bias. If pseudomorphic MODFETs had a high $G_{A\,opt}$, but the same F_{min}, then the model indicates that they would have a higher f_{max} and higher T_d. To make more fair comparisons, the best data from FETs made at the same company with the same gate length and measured at the same frequency are compared where possible. First, 0.2 to 0.3 μm FETs suitable for DBS applications are compared, then 0.1 μm MODFETs are compared. The results are presented in Tables II and III.

The f_{max} of 0.25 μm pseudomorphic MODFETs made by GE is significantly higher than the f_{max} of their conventional MODFETs when biased for maximum gain, as shown in Table II (f_{max} gain) [7]. However, the f_{max} extracted from their 60 GHz noise data (f_{max} noise) is lower for the pseudomorphic MODFET and the 0.25 μm pseudomorphic MODFET has no clear advantage. Although pseudomorphic MODFETs have Indium in their channel, their saturation velocity is not significantly higher and the mobility is lower than GaAs-channel MODFETs because of strain and alloy scattering [87]. The higher peak gain and f_T of pseudomorphic MODFETs is because of the higher modulation efficiency with a higher 2DEG density [8]. At the low drain current density used for lowest noise figure, the higher 2DEG density of pseudomorphic MODFETs has little advantage compared to the conventional

TABLE I
AVERAGE AND PERCENTAGE STANDARD DEVIATION OF PARAMETERS GIVEN IN THE APPENDICES FOR THE DIFFERENT TYPES FETS. CONVENTIONAL (CM), PSEUDOMORPHIC (PM), InP-BASED (InP) MODFETS AND GaAs MESFETS (MES)

FET	T_d (K)		$f_{max} \cdot L_g$ (GHz μm)		$F_{min}/f/L_g$ (dB/GHz/μm)		$G_{A opt} \cdot f \cdot L_g$ (GHz μm)		Id/Width (mA/mm)		L_g (μm)	
Type	Avg.	%	Avg.	%	Avg.	%	Avg.	%	Avg.	%	Avg.	%
CM	566	49.3	28.1	32.2	0.23	36.0	59.0	48.3	57	33.7	0.30	39.0
PM	457	29.7	24.9	30.3	0.24	34.5	47.2	44.5	127	28.0	0.17	43.6
InP	395	35.5	46.3	19.3	0.11	21.4	88.8	40.2	167	0.1	0.16	23.0
MES	520	52.5	23.4	30.0	0.28	38.7	45.5	38.1	78	61.0	0.39	34.9
All	484		30.7		0.21		60.1		107			

TABLE II
COMPARISON OF NOISE FIGURE AND GAIN OF 0.2 TO 0.3 μm CONVENTIONAL MODFETS (CM), PSEUDOMORPHIC MODFETS (PM) AND GaAs MESFETS (MES)

Ref.	FET Type	Company	L_g μm	Freq. GHz	F_{min} dB	$G_{A opt}$ dB	T_d K	f_{max} Noise GHz	f_{max} Gain GHz	$f_m \cdot L_g$ GHz μm	$F_{min}/f/L_g$ dB/GHz/μm	$G_{A opt} \cdot f \cdot L_g$ GHz μm
[7]	CM	GE	0.25	62	2.60	5.7	568	144	171	36.0	0.17	57.6
[7]	PM	GE	0.25	62	2.30	4.0	319	122	231	30.6	0.15	38.9
[9]	CM	Matsushita	0.25	12	0.54	13.1	416	117		29.2	0.18	61.3
[10]	PM	Matsushita	0.2	12	0.75	10.5	332	75		15.0	0.31	26.9
[11]	MES	Matsushita	0.3	12	1.00	7.8	252	49		14.7	0.28	21.7
[12]	MES	Sumitomo	0.3	12	0.72	10.5	317	76		22.9	0.20	40.4

TABLE III
COMPARISON OF NOISE FIGURE AND GAIN OF 0.1 μm GATE LENGTH CONVENTIONAL (CM), PSEUDOMORPHIC (PM) AND InP-BASED (InP) MODFETS

Ref.	FET Type	Company	L_g μm	Freq. GHz	F_{min} dB	$G_{A opt}$ dB	T_d K	f_{max} GHz	I_{ds}/Z mA/mm	$f_{max} \cdot L_g$ GHz μm	$F_{min}/f/L_g$ dB/GHz/μm	$G_{A opt} \cdot f \cdot L_g$ GHz μm
[14]	CM	Toshiba	0.1	18	0.51	10.8	230	138	75	13.8	0.28	21 6
[15]	PM	Toshiba	0.1	18	0.55	14.1	534	195	120	19.5	0.31	46.3
[14]	CM	Toshiba	0.1	40	1.90	5.3	326	97		9.7	0.48	13.6
[15]	PM	Toshiba	0.1	40	1.10	10.5	527	215	150	21.5	0.28	44.9
[16]	CM	GE	0.1	60	2.50	8.4	995	192		19.2	0.42	41.5
[17]	PM	TRW	0.1	93	2.10	6.3	474	246	135	24.6	0.23	39.7
[6]	InP	GE	0.1	94	1.20	7.2	275	333		33 3	0.13	49.3
[6]	InP	GE	0.1	60	0.80	8.9	248	304		30.4	0.13	46.6

MODFET and the lower mobility of the InGaAs channel is probably a disadvantage.

Note that Matsushita has reported the best noise figure and gain at 12 GHz for 0.25 μm conventional MODFETs [9]. However, their pseudomorphic MODFET with a shorter gate length has poorer noise figure, gain and f_{max} [10]. The best pseudomorphic results with a gate length of 0.2 μm (e.g., F_{min} of 0.55 dB at 12 GHz with a $G_{A opt}$ of 11.3 dB [13]) are poorer than the best 0.25 μm conventional MODFET noise figure. It appears that although 0.25 μm pseudomorphic MODFETs have higher peak f_T and f_{max} than 0.25 μm conventional MODFETs, the noise performance appears to be a little worse.

The advantage of pseudomorphic over conventional MODFETs at 0.1 μm gate lengths is shown in Table III. Toshiba's 0.1 μm pseudomorphic MODFETs have higher gain (2.3 dB) than conventional MODFETs at 18 GHz; and at 40 GHz both higher gain (5.2 dB) and lower noise figure (0.8 dB) [14], [15]. The noise and gain figures-of-merit, $G_{A opt} \cdot f \cdot L_g$ and $F_{min}/f/L_g$, degrade more for conventional MODFETs than pseudomorphic MODFETs when the gate length is decreased from 0.25 to 0.1 μm, as shown in Tables II and III. GE's 0.1 μm conventional MODFETs have a high $G_{A opt} \cdot f \cdot L_g$ product (41.5 GHz/μm), but also a high $F_{min}/f/L_g$ (0.42 dB/GHz/μm) [16]. Perhaps the Ge MODFETs were biased at high I_{ds} to obtain high gain at the expense of noise figure. The best 0.1 μm GaAs-based MODFETs are from TRW [17]; their pseudomorphic MODFETs had $F_{min}/f/L_g$ and $G_{A opt} \cdot f \cdot L_g$ products comparable to 0.25 μm conventional MODFETs. A comparison in Table III of 0.1 μm pseudomorphic and InP-based MODFETs at 94 GHz shows that the InP-based MODFETs have significantly lower noise figure (57%) and higher gain. This results from their higher f_{max} and lower T_d [6].

The low-noise drain current densities were calculated wherever possible for the results summarized in the appendices and the average values for each type of FET are

given in Table I. The current densities are significantly different for the three different types of MODFET. The current densities are in the order of: conventional, pseudomorphic, and InP-based MODFETs. The average low-noise bias current densities follow the trends of the optimum current density for maximum gain and maximum 2DEG sheet density.

There are many reasons to expect a range of T_d values for even one FET. These reasons are important for understanding noise figure results, but they are not reviewed in detail here. First, T_d is a function of bias [89]. The drain current used depends on the frequency [20] and applications of the FETs [21]. The second reason for higher values of T_d is that the generator can be tuned for higher gain rather than noise figure. Errors in measuring the minimum noise are a third reason that T_d values can differ [22]–[25].

The final reasons for a range of T_d are source inductance and C_{gd}. These elements do not reduce $F_{\min}$ significantly, but they reduce $G_{A\,\mathrm{opt}}$ and result in a lower $f_{\max}$ and lower effective T_d. Measurements made on-wafer to 18 GHz with automated systems, such as those available from ATN and Cascade Microtech, have very low source inductance. Therefore, on-wafer measurements should have a higher effective T_d and $f_{\max}$ [26] compared to measurement of low-noise hybrid amplifiers that have higher source inductance. C_{gd} per unit gate width has a large range for FETs; typically 0.05 to 0.15 pF/mm. This range of C_{gd} must also contribute to the range of T_d values extracted from measurements. For example, the lowest effective T_d (e.g., 197 to 247 K) for a 0.25 μm T-gate MODFET was found in a FET with a large T-gate top (0.7 μm) and a low aspect ratio; C_{gd} per unit width was 0.19 pF/mm and C_{gs}/C_{gd} was 2.1 [27]. These MODFETs had a $F_{\min}$ at 12 GHz of 0.68 dB, which is typical for 0.25 μm MODFETs (e.g., 0.61 dB), but their $G_{A\,\mathrm{opt}}$ was low, 9.7 dB, compared to typical values (e.g., 12.9 dB).

VI. Discussion

The comparison of the published results with the extrinsic FET noise model suggests the best method to reduce noise figure and increase the available gain is to increase the $f_{\max}$ of FETs at low-noise bias. The techniques for increasing the $f_{\max}$ of an unilateral FET are review first (i.e., improving element in equation 4: f_T, r_{gs}, and G_{ds}), then negative feedback is discussed.

A high f_T is of primary importance for high $f_{\max}$. Fukui's equation also suggests a higher f_T reduces $F_{\min}$ [28], [29]. Higher f_T is achieved with shorter gate lengths (e.g., 0.1 μm) and material with higher carrier velocity (e.g., InGaAs on InP). However, it is important to remember that parasitics must also be reduced to observe all the improvements of intrinsic f_T [33], [38]. To improve f_T at high current densities increasing the saturated velocity is most important. However, the lowest noise figure is observed at low drain currents where the FET is operating closer to the gradual channel mode. Therefore, high mobility is also a key factor for lower noise. There is evidence that mobility is important. First, the difference in performance of MODFETs compared to MESFETs is larger at low temperatures where the MODFETs have much higher mobility [30]. Second, a MODFET fabricated without an undoped spacer between the channel and the supply layer has a higher g_m (because the gate-channel spacing is smaller and the 2DEG sheet density is higher), but the mobility of the 2DEG is lower. As exected, the MODFETs fabricated without a spacer had higher noise figures [31], [32].

Lower input resistance increases the $f_{\max}$ of a FET. This is achieved by reducing the parasitic resistance: the gate and source resistances. Short gate length FETs (L_g less than 0.5 μm) need T shaped gate cross-sections to reduce gate resistance. FETs are designed with many parallel, short fingers to reduce R_g [34]. Source resistance has been reduced with a (1) heavily-doped (N^+) cap layer [35], (2) optimizing epi design for conduction between cap at 2DEG [9], [35], [36] and (3) reducing the gate-source spacing. The minimum spacing is achieved using self-aligned gates [37].

Lower output conductance, G_{ds}, improves $f_{\max}$. The lower G_{ds} and better voltage gain, G_v, of MODFETs compared to MESFETs (e.g., G_v of 25 versus 15) may account for some of the improved noise performance of MODFETs. G_{ds} is probably lower for MODFETs because of heterojunction confinement of the carriers and a high aspect ratio. The importance of output conductance was shown recently with a comparison of normal and inverted pseudomorphic MODFETs [88]. The inverted and normal MODFETs have g_m/G_{ds} ratios of 16.1 and 10.7 respectively, and $f_{\max}$s of 90 GHz and 76 GHz respectively. The lower G_{ds} and higher $f_{\max}$ of the inverted MODFET resulted in a lower $F_{\min}$ of 0.56 dB ($G_{A\,\mathrm{opt}}$ 11.0 dB) compared the normal MODFET, with a $F_{\min}$ of 0.66 dB ($G_{A\,\mathrm{opt}}$ 10.1). The extrinsic T_d values extracted for the inverted and normal MODFETs were similar (267 K and 262 K respectively).

G_{ds} can be reduced and $f_{\max}$ increased with a wider gate recess [91], at the expense of f_T. I am unaware of any reports on how a wide gate recess affects $F_{\min}$, however, it is commonly accepted that a low-noise FET should not have a wide gate recess like a power FET. It is likely that a wide gate recess does not improve $f_{\max}$ and $F_{\min}$ at the bias for lowest noise figure. This is a topic that requires more study.

The simple expression for $f_{\max}$ given in (4) does not include any negative feedback elements. The feedback capacitance C_{gd} reduces $G_{A\,\max}$ and $G_{A\,\mathrm{opt}}$ significantly in most FETs despite having a relatively small value. C_{gd} increases the effective G_{ds} proportional to $\pi C_{gd} f_T$. C_{gd} is reduced by careful gate trough design, passivation, T-gate design and minimization of layout parasitics. When FETs are made with a very large T-gate top to footprint ratio (e.g., 0.5 μm top and 0.1 μm footprint), the $f_{\max} \cdot L_g$ product is small and the associated gain is low because C_{gd} per unit width is large [14], [27]. Increasing C_{gd} does not reduce $F_{\min}$ significantly for low-noise FETs, but it does reduce the associated gain.

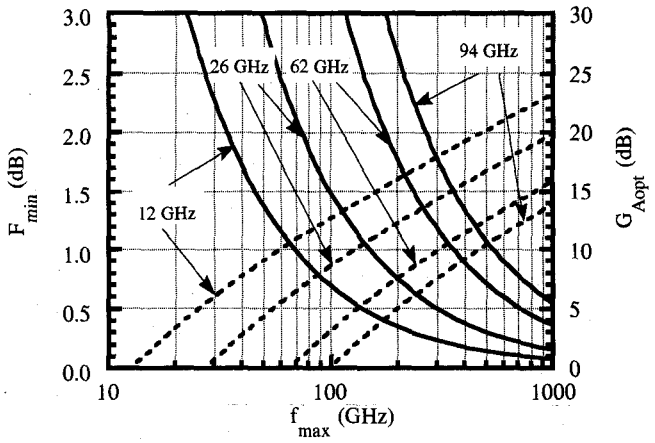

Fig. 6. Plot of the modelled F_{min} and $G_{A\,opt}$ versus f_{max} at frequencies of 12, 26, 60, and 94 GHz. The solid line is F_{min} and the broken line is $G_{A\,opt}$. The effective noise temperatures in the extrinsic FET noise model are T_g of 298 K and T_d of 500 K.

The model can also be used to suggest the device f_{max} necessary to achieve system requirements in noise figure and associated gain. F_{min} and $G_{A\,opt}$ are a function of f_{max} only for a given frequency and fixed (and uncorrelated) T_d (e.g., 500 K) and T_g (e.g., ambient). This concept is shown in Fig. 6 for some common frequencies of interest. For example, if the system requires a minimum noise figure of 2 dB at 94 GHz then f_{max} has to be at least 254 GHz at the low noise bias. From this value one can then design a FET with the gate length (e.g., 0.15 μm) and material type (e.g., InP-based MODFETs) to achieve this f_{max}.

VII. Conclusions

A simple temperature noise model for extrinsic FETs gives a method to compare noise figure and associated gain of different FETs. The model can be used to predict the frequency dependence of the noise figure and associated gain from measurements at a single frequency. The model is simple enough to understand, and the intrinsic model on which it is based is physically reasonable [1]. There are only two essential fitting parameters: T_d and f_{max}. The effective f_{max} and T_d values are extracted directly from the measured F_{min} and associated gain. Experimentally, f_{max} extracted from noise measurements is close to the f_{max} predicted from the circuit model of the extrinsic FET.

A comparison of the model to the literature showed that the extracted T_d values have a limited range of about 300 to 700 K for most extrinsic FETs. The analysis indicates that a InP-based MODFET has significantly lower F_{min} higher $G_{A\,opt}$ than a conventional or a pseudomorphic GaAs-based MODFET of the same gate length. The InP-based MODFETs are better because they have a much higher $f_{max} \cdot L_g$ product.

The model suggests that a lower G_{ds} reduces noise figure and higher voltage gain reduces the Fukui fitting factor, K_f. $G_{A\,opt}$ decreased 3 dB per octave at low frequencies, but the slope increases to 6 dB per octave as the frequency approaches f_{max}. The total output noise power from a FET with the generator tuned for minimum noise figure is almost independent of frequency and the effective total output noise power per Hertz is approximately twice kT_d. This means there are equal noise contributions from the input and output resistors of a FET when the generator impedance is tuned for F_{min}. The temperature noise model suggests that f_{max} is a key parameter for determining noise figure.

Appendix

TABLE A1
Noise Figure Results from the Literature for AlInAs/GaInAs/InP MODFETs

Ref.	Year	Company	L_g μm	Freq. GHz	F_{min} dB	$G_{A\,opt}$ dB	T_d K	f_{max} GHz	I_{ds}/Z mA/mm	$f_{max} \cdot L_g$ GHz μm	$F_{min}/f/L_g$ dB/GHz/μm	$G_{A\,opt} \cdot f \cdot L_g$ GHz μm
[6]	91	GE	0.1	60	0.80	8.9	248	304		30.4	0.13	46.6
[6]	91	GE	0.1	94	1.20	7.2	275	333		33.3	0.13	49.3
[26]	90	GE	0.15	18	0.30	17.2	563	367		55.1	0.11	141.7
[26]	90	GE	0.15	93	1.40	6.6	291	291	167	43.6	0.10	63.8
[43]	90	GE	0.15	18	0.30	17.1	550	363		54.5	0.11	138.5
[43]	90	GE	0.15	60	0.90	8.6	266	280		42.0	0.10	65.2
[43]	90	GE	0.15	94	1.40	6.5	285	291	167	43.6	0.10	63.0
[51]	90	GE	0.15	18	0.30	17.2	563	367		55.1	0.11	141.7
[51]	90	GE	0.15	93	1.40	6.6	291	291		43.6	0.10	63.8
[52]	89	GE	0.15	18	0.30	17.2	563	367		55.1	0.11	141.7
[52]	89	GE	0.15	60	0.90	8.6	266	280		42.0	0.10	65.2
[52]	89	GE	0.15	94	1.40	6.5	285	291		43.6	0.10	63.0
[53]	89	GE	0.15	18	0.50	15.2	619	231		34.7	0.19	89.4
[53]	89	GE	0.15	60	1.20	8.5	371	247		37.1	0.13	63.7
[53]	89	GE	0.15	94	2.10	6.4	485	251		37.7	0.15	61.5
[44]	89	GE	0.15	18	0.30	17.1	550	363		54.5	0.11	138.5
[44]	89	GE	0.15	60	0.90	8.6	266	280		42.0	0.10	65.2
[44]	89	GE	0.15	94	1.40	6.5	285	291		43.6	0.10	63.0
[54]	88	GE	0.25	18	0.50	15.2	619	231		57.8	0.11	149.0
[54]	88	GE	0.25	58	1.20	8.5	371	239		59.7	0.08	102.7
[55]	88	Hughes	0.2	63	1.40	8.5	451	245		49.0	0.11	89.2
[19]	88	Hughes	0.2	60	0.80	8.7	237	297		59.5	0.07	89.0

TABLE A2
NOISE FIGURE RESULTS FROM THE LITERATURE FOR CONVENTIONAL AlGaAs/GaAs/GaAs MODFETs

Ref.	Year	Company	L_g μm	Freq. GHz	F_{min} dB	$G_{A\,opt}$ dB	T_d K	f_{max} GHz	I_{ds}/Z mA/mm	$f_{max} \cdot L_g$ GHz μm	$F_{min}/f/L_g$ dB/GHz/μm	$G_{A\,opt} \cdot f \cdot L_g$ GHz μm
[56]	90	Fujitsu	0.25	30	1.60	7.5	428	99		24.8	0.21	42.2
[37]	88	Fujitsu	0.25	12	0.54	12.1	330	104	60	26.0	0.18	48.7
[5]	87	Fujitsu	0.25	12	0.70	10.4	300	77		19.1	0.23	32.9
[5]	87	Fujitsu	0.25	20	1.00	8.3	282	86		21.6	0.20	33.8
[5]	87	Fujitsu	0.25	30	1.70	6.1	337	83		20.7	0.23	30.6
[57]	84	Fujitsu	0.5	20	1.85	9.0	737	75		37.5	0.19	79 4
[35]	83	Fujitsu	0.4	12	1.08	12.7	854	83	50	33.4	0.23	89.4
[35]	83	Fujitsu	0.4	20	1.70	8.8	627	75	50	30.1	0.21	60.7
[58]	83	Fujitsu	0.5	8	1.30	13.0	1156	54		26.9	0.33	79.8
[58]	83	Fujitsu	0.5	11.3	1.70	11.2	1089	56		28.0	0.30	74.5
[58]	83	Fujitsu	0.5	20	3.10	7.5	1135	55		27.3	0.31	56.2
[59]	83	Fujitsu	0.5	12	1.40	11.0	803	62	50	31.1	0.23	75.5
[60]	89	GE	0.25	8	0.40	15.2	484	114		28.4	0.20	66.2
[60]	89	Ge	0.25	18	0.70	15.0	865	195		48.7	0.16	142.3
[60]	89	GE	0.25	18	0.70	11.5	386	130		32.6	0.16	63.6
[60]	89	GE	0.25	32	1.20	10.0	523	157		39.2	0.15	80.0
[60]	89	GE	0.25	32	1.30	7.5	326	114		28.5	0.16	45.0
[44]	89	GE	0.25	18	0.70	13.2	571	158		39.6	0.16	94.0
[44]	89	GE	0.25	60	1.80	6.4	390	168		42.1	0.12	65 5
[16]	88	GE	0.25	8	0.40	15.2	484	114		28.4	0.20	66.2
[16]	88	GE	0.25	18	0.70	13.8	656	170		42.4	0.16	107.9
[16]	88	GE	0.25	32	1.20	10.0	523	157		39.2	0.15	80.0
[16]	88	GE	0.25	60	1.80	6.4	390	168		42.1	0.12	65.5
[16]	88	GE	0.1	60	2.50	8.4	995	192		19.2	0.42	41.5
[30]	88	GE	0.25	8	0.40	15.0	462	111		27.7	0.20	63.2
[3]	87	GE	0.25	8	0.40	15.2	484	114		28.4	0.20	66.2
[3]	87	GE	0.25	18	0.80	12.5	568	138		34.5	0.18	80.0
[3]	87	GE	0.25	30	1.50	10.0	698	135		33.9	0.20	75.0
[3]	87	GE	0.25	40	1.80	7.5	502	127		31.8	0.18	56.2
[3]	87	GE	0.25	62	2.60	4.4	421	124		31.0	0.17	42.7
[7]	87	GE	0.25	62	2.60	5.7	568	144		36.0	0.17	57.6
[4]	86	GE	0.25	62	2.70	3.8	388	114		28.6	0.17	37.2
[31]	85	GE	0.25	8	0.60	12.9	447	73		18.2	0.30	39.0
[31]	85	GE	0.25	8	0.80	12.5	568	61	55	15.4	0.40	35.6
[31]	85	GE	0.25	18	1.30	8.2	383	70		17.4	0.29	29.7
[61]	85	GE	0.25	18	1.20	11.6	756	106		26.5	0.27	65.0
[61]	85	GE	0.25	30	1.80	9.7	834	123		30.7	0.24	70.0
[61]	85	GE	0.25	40	2.10	7.0	557	114		28.6	0.21	50.1
[62]	87	Hughes	0.25	18	1.00	11.5	590	112		28.1	0.22	63.6
[62]	87	Hughes	0.25	35	1.80	7.2	469	108		26.9	0.21	45 9
[9]	89	Matsushita	0.25	12	0.54	13.1	416	117	50	29.2	0.18	61.3
[27]	88	Mitsubsi	0.25	12	0.68	9.7	247	71	67	17.9	0.23	28.0
[27]	88	Mitsubsi	0.25	18	0.83	7.7	197	78		19.6	0.18	26.5
[63]	88	Mitsubsi	0.25	12	0.68	9.7	247	71		17.9	0.23	28.0
[63]	88	Mitsubsi	0.25	18	0 83	7.7	197	78		19.6	0.18	26.5
[64]	86	NEC	0.5	12	0.95	10.3	420	67	55	33.3	0.16	64.3
[65]	86	NEC	0.5	4	0.34	14.8	370	58		29.2	0.17	60 4
[1]	89	NRAO	0.3	8.5	0.90	10.6	419	50		15.0	0.35	29.3
[25]	89	NRAO	0.25	43	1.50	5.0	221	109		27.3	0 14	34.0
[25]	89	NRAO	0.25	43	2.91	3.7	427	77		19.2	0.27	25 2
[21]	88	NRAO	0.3	8.5	1.03	11.7	640	54		16 1	0.40	37.7
[32]	85	NRAO	0.35	8.5	1.33	8.4	413	33	17	11.7	0.45	20.6
[32]	85	NRAO	0.33	8.5	1.46	9.6	614	37	83	12.2	0.52	25.6
[66]	86	Rockwell	0.5	35	2.00	5.0	328	81	67	40.4	0.11	55.3
[67]	85	Rockwell	0.5	8	1.00	16.1	1701	85		42.4	0.25	163.0
[67]	85	Rockwell	0.5	18	1.80	11.3	1205	89		44.4	0.20	121.4
[68]	86	Sony	0.5	12	0.87	12.5	628	89	40	44.5	0.15	106.7
[69]	86	Sony	0.5	12	0.83	12 5	594	91		45.4	0.14	106.7
[70]	85	Sony	0.8	12	1.47	9.0	540	49	40	38.9	0.15	76.3
[71]	86	Thompson	0.35	12	1.10	13.2	981	88		30.7	0.26	87.8
[71]	86	Thompson	0.35	25	2.00	9.0	823	91		32.0	0.23	69.5
[14]	89	Toshiba	0.1	18	0.51	10.8	230	138	75	13.8	0.28	21.6
[14]	89	Toshiba	0.1	26.6	0.90	8.8	279	127		12.7	0.34	20.2
[14]	89	Toshiba	0.1	40	1.90	5.3	326	97		9.7	0.48	13.6
[72]	86	Toshiba	0.25	12	0.77	11.5	432	83		20.9	0.26	42.4
[73]	86	Toshiba	0.25	12	0.70	11.8	414	90		22.5	0.23	45.4
[73]	86	Toshiba	0.25	18	0.90	9.4	320	92		23.0	0.20	39.2
[73]	86	Toshiba	0.25	26	1.50	6.0	278	74		18.5	0.23	25.9
[74]	85	Toshiba	0.25	12	0.66	11.8	387	92	50	23.0	0.22	45.4
[75]	84	TRW	0.35	15	1.30	9.0	460	64		22.2	0.25	41.7
[75]	84	TRW	0.35	18	1.50	10.5	783	86		30.1	0.24	70.7
[75]	84	TRW	0.35	34	2.70	5.9	630	80		28.0	0.23	46.3
[76]	90	Varian	0.25	18	0.90	13.0	733	139		34 9	0.20	89.8
[77]	89	Varian	0.25	18	0.90	13.0	733	139		34.9	0.20	89.8
[77]	89	Varian	0.25	18	1.40	12.0	1011	105	100	26.2	0.31	71.3
[78]	88	Varian	0.25	18	1.40	12.0	1011	105		26.2	0 31	71.3

TABLE A3
NOISE FIGURE RESULTS FROM THE LITERATURE FOR GaAs MESFETs

Ref.	Year	Company	L_g μm	Freq. GHz	F_{min} dB	$G_{A\,opt}$ dB	T_d K	f_{max} GHz	I_{ds}/Z mA/mm	$f_{max} \cdot L_g$ GHz μm	$F_{min}/f/L_g$ dB/GHz/μm	$G_{A\,opt} \cdot f \cdot L_g$ GHz μm
[79]	90	Avantek	0.2	60	4.00	5.0	987	117		23.3	0.33	37.9
[80]	84	Hughes	0.5	12	1.60	11.0	958	59	117	29.7	0.27	75.5
[81]	82	Hughes	0.6	12	1.30	10.3	621	59	50	35.4	0.18	77.1
[81]	82	Hughes	0.6	18	2.20	7.4	653	53	50	31.9	0.20	59 4
[11]	87	Matsushita	0.3	12	1.00	7.8	252	49	54	14.7	0.28	21.7
[11]	87	Matsushita	0.3	12	1.10	9.5	418	57	54	17.2	0.31	32.1
[82]	90	Mitsubsi	0.4	12	0.87	10.6	407	72	67	28.7	0.18	55.4
[83]	83	NEC	0.5	12	1.70	8.8	627	45	36	22.6	0.28	45.5
[32]	85	NRAO	0.3	8.5	1.43	9.9	33	39	33	11.6	0 56	24.9
[84]	90	Sumitomo	0.3	12	0.72	10.5	317	76		22.9	0 20	40.4
[84]	90	Sumitomo	0.3	18	1.15	8.5	351	75		22.6	0.21	38.2
[12]	90	Sumitomo	0.3	12	0.72	10.5	317	76	100	22.9	0.20	40.4
[12]	90	Sumitomo	0.3	18	1.15	8.5	351	75	100	22.6	0.21	38.2
[85]	90	Sumitomo	0.5	12	1.23	9.0	429	52	193	25.9	0.21	47.7
[86]	85	Toshiba	0.25	18	1.80	9.0	710	68		17.0	0.40	35.7

TABLE A4
NOISE FIGURE RESULTS FROM THE LITERATURE FOR AlGaAs/GaInAs/GaAs PSEUDOMORPHIC MODFETs

Ref.	Year	Company	L_g μm	Freq. GHz	F_{min} dB	$G_{A\,opt}$ dB	T_d K	f_{max} GHz	I_{ds}/Z mA/mm	$f_{max} \cdot L_g$ GHz μm	$F_{min}/f/L_g$ dB/GHz/μm	$G_{A\,opt} \cdot f \cdot L_g$ GHz μm
[39]	89	Comsat	0.35	14	0.90	12.0	582	97		33.8	0.18	77.7
[39]	89	Comsat	0.35	55	3.90	3.5	668	90		31.6	0.20	43.1
[40]	91	Daimler Benz	0.35	12	0.80	12.0	506	87		30.4	0.19	66.6
[41]	90	GE	0.15	18	0.55	15.0	657	216		32.5	0.20	85.4
[41]	90	GE	0.15	60	1.60	7.6	438	201		30.1	0.18	51.8
[41]	90	GE	0.15	94	2.40	5.4	469	215		32.3	0.17	48.9
[42]	90	GE	0.15	18	0.55	15.4	721	227		34.0	0.20	93.6
[42]	90	GE	0.15	60	1.60	7.6	438	201		30.1	0.18	51.8
[43]	90	GE	0.15	18	0.50	15.1	605	228		34.3	0.19	87.4
[43]	90	GE	0.15	60	1.60	7.6	438	201		30.1	0.18	51.8
[43]	90	GE	0.15	94	2.40	5.4	469	215	170	32.3	0.17	48.9
[44]	89	GE	0.15	18	0.55	15.2	688	221		33.2	0.20	89.4
[44]	89	GE	0.15	60	1.60	7.6	438	201		30.1	0.18	51.8
[45]	89	GE	0.1	94	3.00	5.1	619	196	240	19.6	0.32	30.4
[20]	89	GE	0.15	18	0.55	15.2	688	221	53	33.2	0.20	89.4
[20]	89	GE	0.15	60	1.80	6.4	390	168	160	25.2	0.20	39.3
[7]	87	GE	0.25	62	2.30	4.0	319	122		30.6	0.15	38.9
[10]	90	Matsushita	0.2	12	0.75	10.5	332	75	114	15.0	0.31	26.9
[46]	89	Matsushita	0.2	12	0.70	10.4	300	77	100	15.3	0.29	26.3
[13]	90	NEC	0.2	12	0.55	11.3	278	94		18.8	0.23	32.1
[13]	90	NEC	0.2	12	0.68	10.9	328	82		16.5	0.28	29.7
[25]	89	NRAO	0.1	43	1.32	6.7	276	139		13.9	0.31	20.1
[25]	89	NRAO	0.1	43	2.23	6.0	483	108		10.8	0.52	17.1
[88]	91	Oki	0.2	12	0.56	11.0	267	90	100	18.1	0.23	30.2
[88]	91	Oki	0.2	12	0.66	10.1	262	76		15.2	0.28	24 6
[88]	91	Oki	0.2	18	1.01	10.9	520	105		20.9	0.28	44.3
[88]	91	Oki	0.2	18	1.14	9.9	480	89		17.8	0.32	35.2
[47]	90	Toshiba	0.1	18	0.50	13.6	428	192	140	19.2	0.28	41.2
[47]	90	Toshiba	0.1	40	1.60	9.4	663	165		16.5	0.40	34.8
[15]	90	Toshiba	0.1	18	0.55	14.1	534	195	120	19.5	0 31	46.3
[15]	90	Toshiba	0.1	40	1.10	10.5	527	215	150	21.5	0.28	44.9
[48]	91	TRW	0.15	60	1.50	6.1	284	173		25.9	0.17	36.7
[49]	90	TRW	0.1	92.5	2.50	4.7	425	193	82	19.3	0.27	27.3
[17]	90	TRW	0.1	93	2.10	6.3	474	246	135	24.6	0.23	39.7
[36]	87	TRW	0.2	12	0.61	12.6	423	104		20.9	0.25	43.5
[50]	89	Varian	0.1	43	1.30	6.7	271	140		14.0	0.30	20.1

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